CLAIMS

What is claimed is:

1. A method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, comprising:

generating command signals for accessing an integrated circuit component;

accessing data signals for conveying data for the integrated circuit component;

accessing sampling signals for controlling the sampling of the data signals; and

automatically adjusting a phase relationship between the command signals, the data signals, and the sampling signals to calibrate operation of the integrated circuit device.

2. The method of claim 1, wherein the integrated circuit device is a DRAM component.

3. The method of claim 2, wherein the adjusting of the phase relationship is performed by a memory controller coupled to the DRAM component.

4. The method of claim 2, wherein the DRAM component is a DDR DRAM component.

5. The method of claim 4, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component.

6. The method of claim 5, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component.

7. A system for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, comprising:

a controller for generating command signals for accessing an integrated circuit component;

a delay calibrator integrated within the controller and configured to access data signals conveying data for the integrated circuit device and to access sampling signals for controlling the sampling of the data signals, the delay calibrator further configured to automatically adjust a phase relationship between the command signals, the data signals, and the sampling signals to calibrate operation of the integrated circuit device, without requiring a valid initial operating point for the integrated circuit device.

8. The method of claim 7, wherein the integrated circuit device is a DRAM component.

9. The method of claim 8, wherein the DRAM component is a DDR DRAM component.

10. The method of claim 9, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component.

11. The method of claim 10, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component.

12. In a memory controller, a method for finding an operating mode for a DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DRAM component, comprising:

generating command signals for accessing a DRAM component;

accessing data signals for conveying data for the DRAM component;

accessing sampling signals for controlling the sampling of the data signals; and

automatically altering a phase relationship between the command signals, the data signals, and the sampling signals to determine an operating mode of the DRAM component, without requiring a valid initial operating point for the DRAM component.

13. The method of claim 12, further comprising:

performing a coarse calibration by altering the phase relationship in accordance with a large step interval to find the operating mode of the DRAM component; and

performing a fine calibration by altering the phase relationship in accordance with a small step interval to optimize the operating mode of the DRAM component.

14. The method of claim 13, further comprising:

configuring the memory controller to operate with the DRAM component in accordance with an optimal operating mode, wherein the optimal operating mode is determined via the fine calibration.

15. The method of claim 12, wherein the DRAM component is a DDR DRAM component.

16. The method of claim 15, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component.

17. The method of claim 16, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component.

18. A computer readable media for finding an operating mode for a DDR DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DDR DRAM component, the media storing computer readable code which when executed by a memory controller causes the memory controller to implement a method comprising:

generating command signals for accessing a DDR DRAM component;

accessing DQ signals for conveying DQ for the DDR DRAM component;

accessing DQS signals for controlling the sampling of the DQ signals; and

automatically altering a phase relationship between the command signals, the DQ signals, and the DQS signals to determine an operating mode of the DDR DRAM component, without requiring a valid initial operating point for the DRAM component.

19. The computer readable media of claim 18, further comprising:

performing a coarse calibration by altering the phase relationship in accordance with a large step interval to find the operating mode of the DDR DRAM component; and

performing a fine calibration by altering the phase relationship in accordance with a small step interval to optimize the operating mode of the DDR DRAM component.

20. The computer readable media of claim 19, further comprising:

configuring the memory controller to operate with the DDR DRAM component in accordance with an optimal operating mode, wherein the optimal operating mode is determined via the fine calibration.

21. In a memory controller, a method for finding an operating mode for a DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DRAM component, comprising:

generating command signals for accessing a DRAM component;

accessing data signals for conveying data for the DRAM component;

accessing sampling signals for controlling the sampling of the data signals; and

automatically altering a phase relationship between the command signals, the data signals, and the sampling signals to determine an operating mode of the DRAM component, wherein the DRAM component inoperable at a specified initial operating point.

22. In a memory controller, a method for finding an operating mode for a DRAM component coupled to a PCB (printed circuit board) by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DRAM component, comprising:

generating command signals for accessing a DRAM component;

accessing data signals for conveying data for the DRAM component;

accessing sampling signals for controlling the sampling of the data signals; and

automatically altering a phase relationship between the command signals, the data signals, and the sampling signals transmitted via a PCB to determine an operating mode of the DRAM component, wherein the DRAM component is inoperable at a specified initial operating point.